SPC1185 Datasheet

32-bit ARM® Cortex-M4F based MCU with 16-channel PWM, 23-channel 14-bit ADC, 3 PGAs with comparators

Features

- 32-bit ARM® Cortex-M4F CPU
  - Single-precision floating point unit (FPU)
  - Up to 240MHz clock frequency
- Embedded memory
  - Up to 512KB QSPI Flash (ECC protection), support execution in place with 16KB read cache
  - 256-byte OTP Flash
  - Up to 256KB RAM with ECC protection
- Clock, reset and power management
  - Single 3.3V power supply
  - Power-on reset and brown-out under-voltage or over-voltage detector (BOD)
  - 4~32MHz crystal oscillator
  - Internal 32MHz oscillator (trimmed)
  - Internal backup-safety 32MHz oscillator
  - Internal PLL for flexible clocking
- 3 14-bit ADCs (23 external input channels)
  - 140ns conversion time
  - Input range: 0 ~ 3.339V
  - Differential sampling
  - Open/short detection on external input
  - Multi-channel simultaneous sampling
- Temperature sensor
- 3 PGAs
  - Programmable gain
    Single-ended: 1/2/4/8/12/16/24/32
    Differential: 2/4/8/16/24/32/48/64
  - Typical settling time: 600ns
- 16 analog comparators
  - Optional output digital filter
  - Provide five 10-bit DACs and a 12-bit DAC to generate the reference
  - Voltage out of range protection
  - Phase comparison

QFN56 (6 x 6 x 0.85mm, 0.35mm pitch)

- 8 PWMs
  - 16-channel flexible waveform output
  - Multi-event to trigger ADC conversion
- 8 ECAPs (enhanced capture module)
  - Capture input can be programmed as any one of the GPIO channels
  - Four 32-bit capture registers
  - Can be used as auxiliary PWM
- 2 EQEP
  - 32-bit counter
  - Support CW/CCW mode, quadrature clock mode, and direction count mode
  - Event based count latch and reset
- 24-bit SysTick timer
- 2 independent 32-bit watchdog timers
- 6 32-bit general-purpose timers
- 2 DMA controllers
  - Up to 16 channels
- Up to 48 GPIOs
  - Independent control for pull-up, pull-down, input deglitch filter, and output strength
- Communication interface
  - 2 CAN/FDACANs, 4 UART/LINs, 3 SPIs, 3 I^2Cs
- Debug interface
  - Support SWD (default) and JTAG
- Security and safety
  - 1 CRC, 1 AES, 64-bit device UID
- Operation temperature
  - Junction temperature：-40 ~ +125 °C
  - Ambient temperature：-40 ~ +105 °C

Table 1-1: SPC1185 device feature and peripheral resources

Item	SPC1185ZAPI56
Max CPU frequency	240MHz
Flash main region(QSPI interface)	512KB (ECC enabled by default)
Flash read cache	16KB
Flash OTP	256 byte
RAM overall volume	256KB
RAM region 0	128KB, up to 240MHz with 0 wait cycle
RAM region 1	128KB, up to 120MHz with 0 wait cycle (1 wait cycle at 240MHz)
GPIOs	48
Analog input channel	23
14-bit ADC	3
Temperature sensor	1
PGA	3
Analog comparator	16
10-bit DAC	5
12-bit DAC	1
DAC output buffer	2
PWM Output channel	8 16
ECAP	8
EQEP	2
General purpose timer	6
Watchdog timer	2
DMA channel	16
UART/LIN	4
QSPI	1 (Used for in-package Flash communication)
SPI	3
I2C	3
CAN / FDCAN	2
CRC	1
AES	1

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Revision history

Version	Date	Author	Status	Changes
A/0	2023-08-16	X. Yu	Outdated	1. Initial release.
C/0	2024-12-09	J. Zhou	Outdated	1. Update Table 1-1 to modify the number of GPIOs for SPC1185API56 to 48, and the number of GPIOs for SPC1185API52 to 44. 2. Update the error in Figure 1-1. The total number of Dacs should be 6. 3. Update the pin arrangement of QFN56 package in Section 3.1, remove GPIO15, add a VCAP12 pin, and change the corresponding capacitor placement scheme. 4. Update the pin arrangement of QFN52 package in Section 3.2, remove GPIO15, add a VCAP12 pin, and change the corresponding capacitor placement scheme. 5. Delete GPIO15 in Section 3.4. 6. Remove ANA_IN15 from Section 3.5. 7. Delete the engineering sample information and ANA_IN15 in Section 3.7 and Section 3.8. 8. Update the current values in Section 5.4. 9. Explain that the timing characteristics of the interface in Section 5.15 are guaranteed by the design according to the condition of 15pF pin capacitance. 10. Update the values of electrical sensitivity properties in Section 5.16. 11. Update Table 7-1 to add product information. 12. Add a description of the performance of the DAC to generate waveforms. 13. Update product package thermal resistance characteristics. 14. Modify the adaptation standard of UART module.
C/1	2025-09-16	J.Zhou	Outdated	1. Add the pin information for the QFN56 (6×6mm) package. 2. Modify Table 5-6. 3. Modify Table 5-16 and Table 5-17.
C/2	2025-12-01	J.Zhou	Outdated	1. Delete QFN56 (8×8mm) and QFN52 packages. 2. Indicate that enabling/disabling ECC does not affect the total Flash capacity. 3. Modify Figure 4-1.
C/3	2025-12-05	J.Zhou	Released	1. Add EQEP module.

Terms or abbreviations

Terms or abbreviations	Description
MCU	Microcontroller Unit
LDO	Low Dropout Regulator
ECC	Error Correction Code
DMAC	Direct Memory Access Controller

1 Device overview

SPC1185 is a high performance and integration system-on-chip (SoC) microcontroller. As shown in Figure 1-1, SPC1185 incorporates a 32-bit high-performance ARM® Cortex-M4F core with a programmable clock up to 240MHz, in-package 512KB QSPI Flash (supports execution in place with 16KB read cache) and 256KB RAM, and extensive range of enhanced I/Os and peripherals.

SPC1185 offers 2 direct memory access controllers (DMAC) with overall 16 channels. They are used to release the CPU resources and provide high-speed data transfer between memories, peripherals, and memory-peripheral combinations.

SPC1185 offers 3 differential 14-bit ADCs, 3 PGAs, 8 enhanced PWMs, 8 ECAPs, 2 EQEPs, 6 general purpose 32-bit timers, as well as standard and advanced communication interface: 4 UART/LINs, 3 I^2Cs, 3 SPIs, 2 CAN/FDCANs. All these features make SPC1185 ideal for motion control applications.

SPC1185 operates from a single 3.3V±10% power supply, with the junction temperature from -40°C to 125°C. The package type can be 56-pin QFN.

Figure 1-2 shows the clock tree of SPC1185, with the maximum clock frequency annotated for each peripheral.

Figure 1-1: SPC1185 block diagram

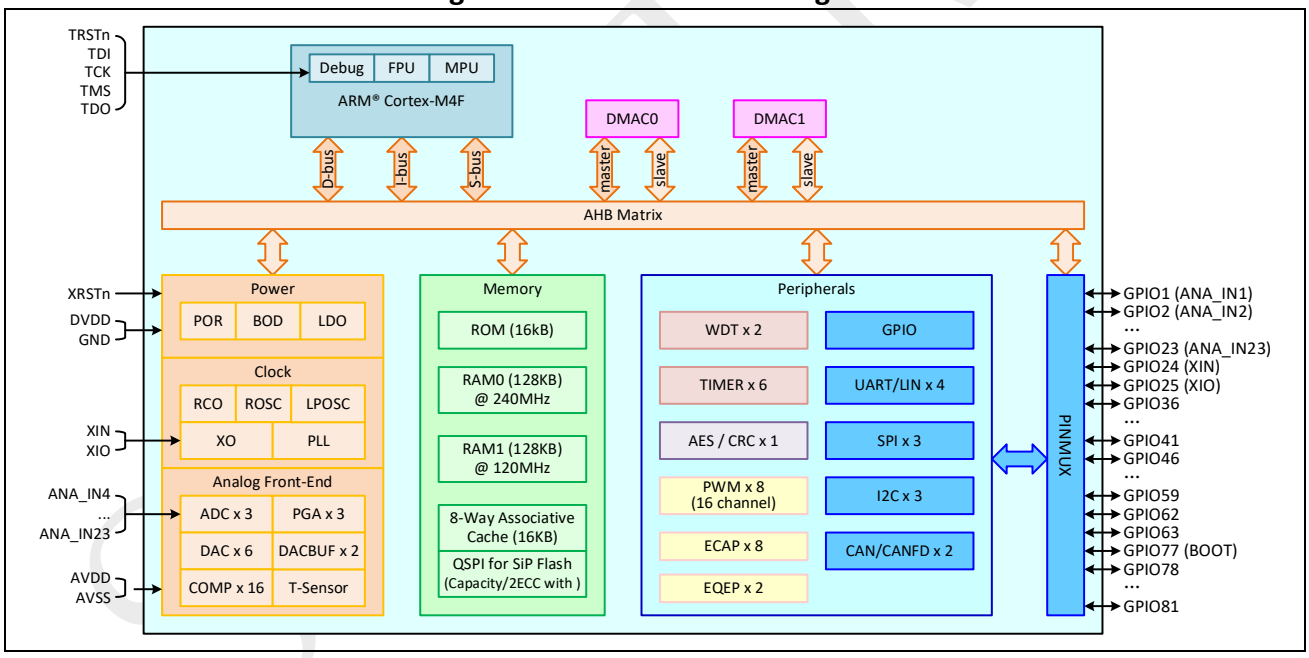
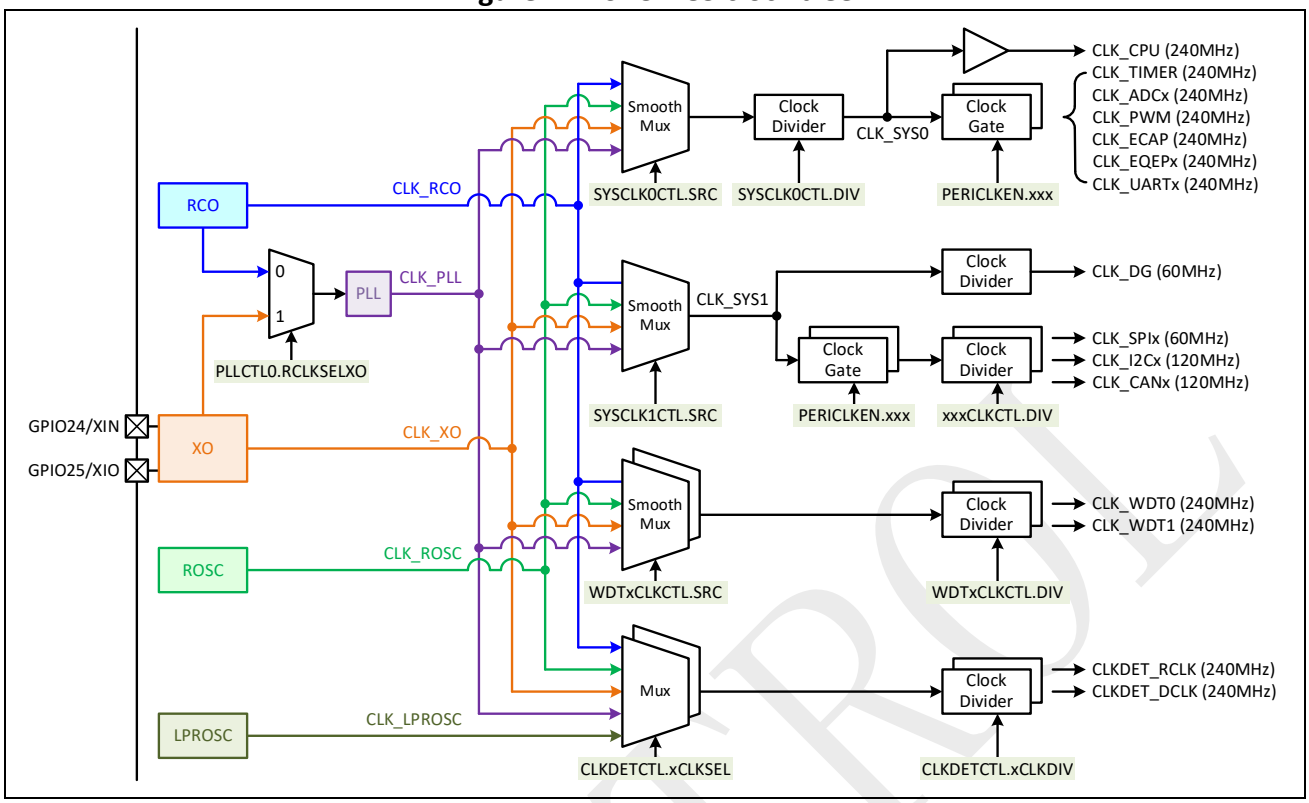


Figure 1-2: SPC1185 clock tree



2 Feature description

2.1 ARM® Cortex-M4F core

SPC1185 integrates a full-feature ARM® Cortex-M4F core that can run up to 240MHz. It supports single-precision floating-point process unit (FPU) and memory protection unit (MPU). It is compatible with all ARM® tools and software.

2.2 Debug interface (SWJ-DP)

The embedded ARM® SWJ-DP interface consists of JTAG and SWD debug interfaces. They are connected to the I/O as shown in Table 2-1. The default mode is SWD with SWV enabled.

Table 2-1: Pin function of debug interface

Pin	SWD mode with SWV	SWD mode without SWV	JTAG mode
GPIO78	User defined function	User defined function	TDI
GPIO79	SWV [1]	User defined function	TDO
GPIO80	SWD	SWD	TMS
GPIO81	SWCK	SWCK	TCK

[1] Function of GPIO79 can be configured via bit-24 of ARM® Cortex-M4F internal register located at 0xE000EDFC (CoreDebug->DEMCR): 1 - SWV output, 0 - User defined function.

2.3 Embedded RAM

SPC1185 offers up to 256KB embedded RAM to store the data and the code. It is implemented into 2 regions as below:

- RAM0
  - 128KB volume, accessed via 0x1FFA0000 ~ 0x1FFBFFFF or 0x20000000 ~ 0x2001FFFF DMA can only access RAM0 via 0x1FFA0000 ~ 0x1FFBFFFF
  - Support up to 240MHz access with 0 wait cycle
- RAM1
  - 128KB volume, accessed via 0x1FFC0000 ~ 0x1FFDFFFF
  - Support up to 120MHz access with 0 wait cycle (1 wait cycle at 240MHz)

ECC protection is adopted for all RAMs (It does not affect the effective RAM volume for the user). ECC error can be programmed to trigger interrupt or reset.

2.4 In-package Flash

SPC1185 offers up to 512KB in-package Flash to store the data and the code. It is accessed via QSPI module. It supports execution in place (XIP) with 16KB read cache to enhance the read speed. Additionally, the ECC function is enabled by default in the chip. Users can choose to keep it enabled or disable it according to their actual needs, and this operation does not affect the total Flash capacity. ECC errors can be configured to trigger either an interrupt or a reset.

The SDK of SPC1185 provides function library to facilitates users in performing operations such as reading, erasing, and programming on the Flash.

2.5 Nested vectored interrupt controller (NVIC)

SPC1185 embeds a nested vectored interrupt controller. It can handle up to 107 maskable interrupt channels (not including the 16 interrupts of Cortex-M4F) and 16 programmable priority levels. It provides features below:

- Closely coupled NVIC gives low-latency interrupt processing.
- Interrupt entry vector table address passed directly to the core.
- Processing of late arriving higher priority interrupts.
- Support for tail-chaining.
- Support for lazy-stacking.
- Context restored on interrupt exit with no instruction overhead.

2.6 External interrupt/event controller

SPC1185 provides a flexible external pin interrupt or event trigger mechanism. Any GPIO pin can be programmed as an external interrupt or event trigger source. Overall, 6 maskable interrupts are supported as below.

- No. 1 interrupt: Specified level is detected on any pin within GPIO4 ~ GPIO25.
- No. 2 interrupt: Specified level is detected on any pin within GPIO36 ~ GPIO63.
- No. 3 interrupt: Specified level is detected on any pin within GPIO77 ~ GPIO81.
- No. 4 interrupt: Specified edge is detected on any pin within GPIO4 ~ GPIO25.
- No. 5 interrupt: Specified edge is detected on any pin within GPIO36 ~ GPIO63.
- No. 6 interrupt: Specified edge is detected on any pin within GPIO77 ~ GPIO81.

In addition, it can also trigger non-maskable interrupt (NMI) when the specified edge on the specified GPIO pin is detected.

2.7 Power supply and reset

SPC1185 supports single 3.3V power supply for the I/Os, internal regulators, and analog modules. **The slew rate should be below $1.5x10^4$ V/s**.

The built-in 1.2V low dropout regulator (LDO) provides power for digital and some analog circuits.

The internal power-on reset (POR) circuit ensures the power-up sequencing requirements. Additionally, the XRSTn pin can also be used to reset the digital logic (XRSTn keeps low for ~500us) or even the entire power system (XRSTn keeps low for ~8.2s).

SPC1185 supports the following two low-power modes:

- Stop mode
  - The main clock and all peripheral clocks are turned off, and only a low-frequency 128kHz clock is used to process wake-up requests.
  - The registers and RAM retain their contents.
  - Wake up due to timeout or by an I/O pin (the pin and the active level can be configured).
  - After waking up, the software can continue execution from the point where it entered the stop mode.

- Sleep mode
  - Turn off the internal power, clocks, and all peripherals on the chip, with all pins in an input high-impedance state.
  - It can be configured to wake up with a specified level on GPIO10 or GPIO11.
  - The startup process after waking up is the same as the power-up cold startup process.

2.8 Brown-out detector (BOD)

SPC1185 has built-in brown-out detector for monitoring the 3.3V and 1.2V power supply. An over-voltage event is generated when the voltage exceeds the preset upper threshold, and an under-voltage event is generated when the voltage falls below the preset lower threshold. Users can configure these events to trigger a non-maskable interrupt (NMI) or a reset.

2.9 Clock

After power-up, SPC1185 uses the factory-calibrated 32MHz internal oscillator as the clock source by default. Users can switch to a crystal oscillator clock or a phase-locked loop (PLL) clock through software. The built-in PLL can select either the crystal oscillator clock or the 32MHz internal oscillator as the input reference to generate a clock signal ranging from 25MHz to 240MHz.

With the clock source selection, enable control, and division control as shown in Figure 1-2, a flexible clock tree can be achieved.

2.10 Boot mode

After reset, SPC1185 executes a bootloader located in ROM and supports two boot modes as described in Table 2-2.

- If GPIO77 is detected as low upon power-on reset or XRSTn pin reset, in-system programming (ISP) mode is entered. The bootloader reprograms the Flash or RAM via UART interface. During this process, GPIO62 is configured as UART0_TXD, and GPIO63 is configured as UART0_RXD.
- For all other cases, the device enters normal startup mode, and the bootloader jumps to the starting address in Flash (0x1000 0000) to begin execution.

Table 2-2: Boot mode

GPIO77	Reset source	Boot mode
0	Power on reset	ISP mode: GPIO62 is used as UART0_TXD GPIO63 is used as UART0_RXD
0	XRSTn pin reset	
0	ARM® CPU system reset request [1]	Normal startup mode: Start program execution from Flash
0	Power over-voltage/under-voltage	
0	PLL unlock / Clock detection error report	
0	ROM/RAM/Flash ECC error	
0	Watchdog timer timeout	
1	Any reset	

[1] When GPIO77 is detected as low after ARM CPU system reset, the engineering sample enters ISP mode, while the final product will enter normal startup mode.

2.11 General-purpose IOs (GPIO)

SPC1185 offers up to 48 multi-purpose GPIO pins. Each GPIO pin can be configured by software as input, as output or as peripheral alternate function. It provides following features:

- Each pin can be configured by software as input, as output or as peripheral alternate function.

- Each pin has a programmable digital input deglitch filter.
- Each pin can be configured as external interrupt or event trigger source. The trigger mechanism can be specified level or edge.
- GPIO4~GPIO25 are pure 3.3V I/O pins. GPIO36~GPIO81 support 3.3V output and tolerate up to 5V input.

2.12 Direct memory access controller (DMAC)

SPC1185 includes 2 DMA controllers, providing a total of 16 channels for managing memory access requests from peripherals. It provides following features:

- 16 independently configurable channels, each supporting a 16 x 32-bit FIFO.
- Support for transfers between memories, peripherals, and memory-peripheral combinations.
- Source and destination addresses can be configured as incremental, decremental, or fixed.
- Support for single-block transfers with configurable sizes, up to a maximum of 4095 words (32 bits).
- 27 optional hardware handshake interfaces.

2.13 General purpose timers

SPC1185 includes 6 identical general-purpose timers with the following features:

- Independent functional clock enable control, with the same maximum clock frequency as CPU.
- 32-bit auto-reload down-counters.
- Generate interrupt request, ADCSOC event and PWMSYNC event when the counter reaches zero.
- Supports 4 operating modes
  - General timer: Periodic down-counter.
  - Gated timer: Down-counter enabled by external input level.
  - Event counter: Down-counter upon external input edge.
  - Event capture: Down-counter with timestamp latched upon external input edge.

2.14 Watchdog timer

SPC1185 includes 2 identical watchdog timers with the following features:

- Independent clock source, clock dividing, and clock enable control, with the same maximum clock frequency as CPU.
- 32-bit auto-reload down-counter.
- Generate interrupt request when the counter reaches zero.
- Generate reset request when the counter reaches zero and the interrupt flag is already set.
- Can be frozen or free running when the CPU is in halted or lockup state.

2.15 SysTick Timer

There is a SysTick timer embedded in ARM® Cortex-M4F. It is dedicated for OS, but could also be used as a standard down-counter with following features:

- 24-bit down-counter with auto-reload capability.

- Generate maskable system interrupt request when the counter reaches zero.

2.16 UART

SPC1185 includes 4 UART modules with following features:

- Independent functional clock enable control, with the same maximum clock frequency as CPU.
- 5 - 8 data-bit.
- Even, odd, fixed or no parity-bit.
- Support 1 and 1.5 or 2 stop-bit.
- Support baud-rate up to 1/16 functional clock frequency.
- Auto baud-rate detection.
- 64-byte transmit FIFO and 64-byte receive FIFO with DMA support.

Dedicated hardware is also implemented in each UART to enable LIN features as below:

- Compatibility with LIN 2.1.
- Configurable baud rate.
- Identification masks for message filtering.
- Hardware processing on break field, sync-byte field, PID field, data field and checksum field.
- Response length can be defined by bit 5 and bit 4 of the PID field, or by register control.
- Programmable classic checksum mode or enhanced checksum mode.

2.17 SPI

SPC1185 includes 3 SPI modules with following features:

- Independent functional clock enable and dividing control, with clock frequency up to 60MHz.
- Communication data rate up to 30Mbps (Maximum serial interface clock frequency is 30MHz).
- Support full-duplex synchronous serial communication.
- Master or slave operation.
- Programmable frame length and format.
- Programmable bit sequence (MSB first or LSB first).
- Programmable clock polarity and phase.
- 16 x 32-bit transmit FIFO and 16 x 32-bit receive FIFO with DMA support.

2.18 QSPI

SPC1185 includes a QSPI module to access the in-package Flash with following features:

- Same functional clock as the CPU.
- Serial interface clock is divided down from CPU clock with programmable dividing ratio.
- Support standard SPI, dual/quad output read, dual/quad I/O communication.
- Programmable clock polarity and phase.

- 64-byte transmit FIFO and 64-byte receive FIFO with DMA support.

2.19 I²C

SPC1185 includes 3 I²C modules, which comply with the general I²C protocol with following features:

- Independent functional clock enable and dividing control, with clock frequency up to 120MHz.
- 4 speed modes
  - Standard mode: Up to 100Kbps.
  - Fast mode: Up to 1Mbps.
  - High-speed mode: Up to 3.4Mbps.
  - Ultra-fast mode: Up to 5Mbps.
- Master or slave operation.
- 7-bit or 10-bit addressing.
- Combined 7-bit and 10-bit addressing.
- Support clock stretching.
- Support transmission abort detection.
- 16-byte transmit FIFO and 16-byte receive FIFO with DMA support.

2.20 CAN

SPC1185 includes 2 CAN modules with following features:

- Independent functional clock enable and dividing control, with clock frequency up to 120MHz.
- Compatible with ISO-11898-1:2015 specification, whose frame format is called classical CAN and ISO-FDCAN.
- Compatible with Bosch CAN2.0B specification.
- Compatible with Bosch FDCAN V1.0 specification, whose frame format is called NONISO-FDCAN.
- Support bus-off recovery.
- Support automatic message re-transmission after transmission failure.
- Support restricted mode.
- Support monitor mode.
- Support test mode.
- Support 64 mailboxes with independent message identifier mask for each mailbox.
- Support automatic remote frame handling.
- Support CAN bus error recording.
- Support 32-bit timestamp.

Note	The CAN module itself in SPC1185 does not support wake-up function. Users need to select a CAN PHY that supports wake-up function and connect the CAN PHY wake-up signal to the GPIO pin SPC1185 to implement the CAN wake-up function.

2.21 ADC

SPC1185 includes 3 14-bit analog-to-digital convertors with following features:

- 14-bit resolution.
- 140 ns conversion time.
- 1 differential sampler for each ADC.
- Analog input range: 0 ~ 3.339V.
- Internal 1.2V reference.
- Analog input can be from 23 external input, temperature sensor, internal power supply or the PGA output.
- External input open and short detection.
- Independent clock enable control for the logic, with the same maximum clock frequency as CPU.
- 8 conversion control channels with independent trigger source, analog input, sample time, conversion time, averaging control, and end-of-conversion (EOC) event generation.
- Conversion priority arbitration.
- Support following events to trigger the start-of-conversion (SOC) request.
  - Software force
  - EOC event
  - PWM SOC signal
  - TIMER SOC signal
  - External request from the I/O pins
- 4 post-processing units (PPUs) for each ADC.
  - Measure the latency from the SOC request to the start of the actual sample and conversion.
  - Comparison with a reference value, where the magnitude of the reference value and the polarity of the comparison are configurable.
  - Out-of-boundary (programmable threshold) and zero-crossing detection on the comparison result. The corresponding events can trigger CPU interrupts or PWM trip-zone.
- DMA support to access the conversion result.

Please refer to Table 5-10 for more characteristics of ADC.

2.22 PGA

SPC1185 includes 3 programmable gain amplifiers with following features:

- Independent input source selection for each PGA:
  - From external input via the 23 I/Os (GPIO4 ~ GPIO23).
  - From internal temperature sensor or DAC output.
- Programmable gain (G_{PGA})
  - Single-ended mode (MODE = 5, 6, 7): 1, 2, 4, 8, 12, 16, 24, 32.
  - Differential sensor mode (MODE = 3): 1, 2, 4, 8, 12, 16, 24, 32.
    The output common-mode voltage is equal to the input common-mode voltage.
  - Differential motor mode (MODE = 1, 2): 2, 4, 8, 16, 24, 32, 48, 64.
    The output common-mode voltage is equal to the positive or negative input terminal.

- Maximum input differential voltage: ±3.339V / G_{PGA}.
- Settling time: 220 ns ~ 2.2 us.
- The output can be directly connected to a 14-bit high-speed ADC.

Please refer to Table 5-11 for more characteristics of PGA.

2.23 Temperature sensor

SPC1185 includes a temperature sensor with following features:

- Generates a voltage varying linearly with temperature and internally connected to the ADC input.
- Measurement precision: LSB of the 14-bit ADC (refer to Section 2.21) corresponds to 1.73°C.
- Measurement accuracy: ±6 °C.
- Measurement range: -40 ~ 125°C.

2.24 Analog comparator (COMP)

SPC1185 includes 16 high-speed comparators. Each comparator use the internal DAC as reference to monitor whether the PGA inputs or outputs exceed the threshold. A DAC can be used to generate a static voltage as a threshold for the somparator, but does not guarantee the performance of the waveform. Its features are as follows：

- Rail-to-rail input.
- Offset is below 10mV.
- 50 ns typical response time.
- Programmable hysteresis.
- Output digital filtering.
- Support phase comparison.
- Out of boundary (programmable upper and lower threshold) comparison, and the result can trigger PWM trip-zone.
- Include 5 10-bit DACs and a 12-bit DAC, to generate the upper and lower threshold.
  - Output voltage for 10-bit DAC: V_{AVDD} / 1024 x Code
  - Output voltage for 12-bit DAC: V_{AVDD} / 4096 x Code
- Include 2 DAC output buffer.
  - DAC buffer 0 can output to GPIO12 from DAC0~DAC3.
  - DAC buffer 1 can output to GPIO13 from DAC4~DAC5.

Please refer to Table 5-12 for more characteristics of analog comparators. Please refer to Table 5-13 and Table 5-14 for more characteristics of DACs. Please refer to Table 5-15 for more characteristics of DAC buffer.

2.25 ECAP

SPC1185 includes 8 ECAP modules with following features:

- Independent functional clock enable control, with the same maximum clock frequency as CPU.
- Each GPIO can be configured as capture pin.
- 32-bit time base counter.
- 4 x 32-bit time-stamp capture register.
- 4-stage sequencer that is synchronized to external events.
- Independent edge polarity (rising or falling edge) selection for all 4 capture events.
- Each capture event can trigger CPU interrupt.

2.26 PWM

SPC1185 includes 8 PWM modules with 16 output channels. It can generate flexible pulse-width modulated waveform without the involvement of the CPU. Its features are as follows:

- Independent functional clock enable control, with the same maximum clock frequency as CPU.
- Dedicated 16-bit time-base counter with period and frequency control.
- Each PWM module can generate 2 outputs with single-edge operation, dual-edge symmetric operation and dual-edge asymmetric operation.
- All events can trigger CPU interrupts and ADC start of conversion request.
- Programmable inter-PWM phase relationship (lead or lag) control.
- Dead-band generation based on independent delay for rising-edge and falling-edge.
- Support cycle-by-cycle or one-shot trip-zone condition triggered by following events:
  - 5 independently configured signals from the GPIO pins.
  - Clock error.
  - CPU enters lockup or halted state.
  - Following events after digital compare and blanking
    Trip-zone request from analog comparator output with optional filtering.
    Trip-zone request from ADC post-processing unit.
    5 independently configured signals from the GPIO pins.
- A trip-zone condition can force either high, low, or high-impedance status at PWM outputs.

2.27 EQEP

SPC1185 includes 2 enhanced quadrature encoder pulse (EQEP) modules with following feature:

- Independent functional clock enable control, with the same maximum clock frequency as CPU.
- Filtering and polarity selection on external A/B/Z/S input.
- Support 4 32-bit decoding count modes:
  - Quadrature clock mode
  - Bidirectional count mode
  - Unidirectional count mode

  - Clockwise/Counterclockwise (CW/CCW) count mode
- Flexible position count reloading, reset, and latch for position measurement.
- Edge capture and unit time base latch for speed or frequency measurement.
- Watchdog timer for stall detection.

2.28 Cyclic redundancy check (CRC)

SPC1185 includes a hardware CRC calculation unit. It is used to verify the integrity for data transmission or storage with following features:

- Support parallel bit stream input in 8-bit or 32-bit.
- Support up to 2^{32}-byte data for CRC calculation.
- Support 8 CRC standard polynomials.

2.29 Advanced encryption standard (AES)

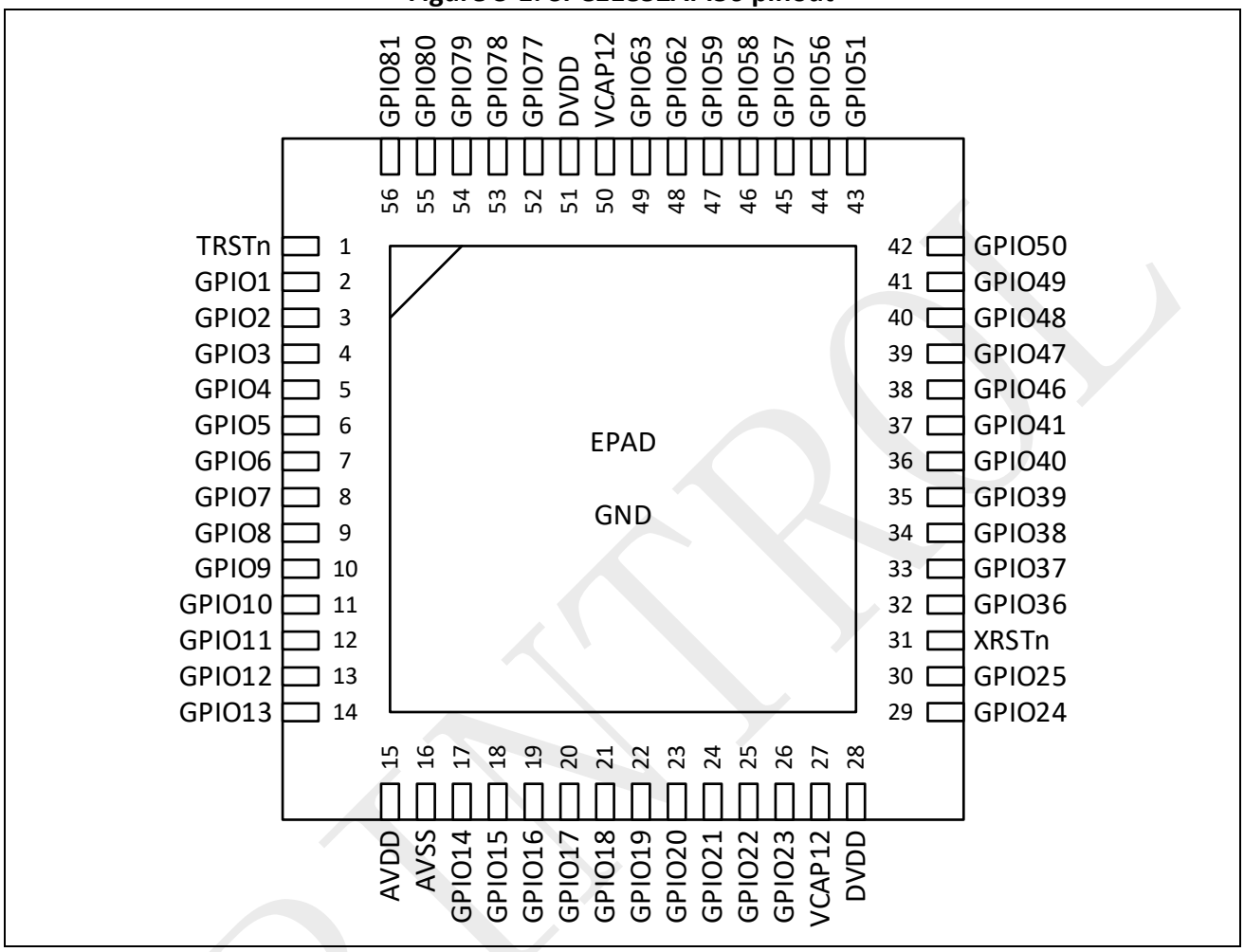
SPC1185 includes an AES module to provide fast hardware encryption and decryption services with following features:

- Support up to 5 block cipher modes: ECB, CBC, CTR, CCM, MMO.
- Verification and error indication for the configuration of each mode.
- Support 128-bit, 192-bit, and 256-bit key.
- 4 x 32-bit input FIFO and 4 x 32-bit output FIFO.

3 Pinout and channel description

3.1 QFN56（6mm x 6mm）

Figure 3-1: SPC1185ZAPI56 pinout



[1] The figure shown above is the top view of the package.

[2] The two VCAP12 pins do not need to be connected together on the PCB. All DVDD and AVDD pins should be connected on the PCB.

[3] When TRSTn pin is high, GPIO78~GPIO81 may be used as shown in Table 2-1.

Table 3-1: SPC1185ZAPI56 pin definitions

Pin	Type	Signal	Sub-type[1]	Description
1	3.3V I/O 5V tolerance	TRSTn	I	Reset CPU debugging logic at low level, and configure GPIO78 to GPIO81 pin function according to Table 2-1 at high level. Internal pull down to DVSS.
2	3.3V I/O	GPIO1	I/O	General purpose input/output 1
		ANA_IN1	AI	Analog input channel 1
3	3.3V I/O	GPIO2	I/O	General purpose input/output 2
		ANA_IN2	AI	Analog input channel 2
4	3.3V I/O	GPIO3	I/O	General purpose input/output 3
		ANA_IN3	AI	Analog input channel 3
5	3.3V I/O	GPIO4	I/O	General purpose input/output 4
		ANA_IN4	AI	Analog input channel 4
6	3.3V I/O	GPIO5	I/O	General purpose input/output 5
		ANA_IN5	AI	Analog input channel 5
7	3.3V I/O	GPIO6	I/O	General purpose input/output 6
		ANA_IN6	AI	Analog input channel 6
8	3.3V I/O	GPIO7	I/O	General purpose input/output 7
		ANA_IN7	AI	Analog input channel 7
9	3.3V I/O	GPIO8	I/O	General purpose input/output 8
		ANA_IN8	AI	Analog input channel 8
10	3.3V I/O	GPIO9	I/O	General purpose input/output 9
		ANA_IN9	AI	Analog input channel 9
		PWM_SOCA	O	PWM_SOCA output monitor
11	3.3V I/O	GPIO10	I/O	General purpose input/output 10
		ANA_IN10	AI	Analog input channel 10
		PWM_SOCB	O	PWM_SOCB output monitor
12	3.3V I/O	GPIO11	I/O	General purpose input/output 11
		ANA_IN11	AI	Analog input channel 11
		PWM_SOCC	O	PWM_SOCC output monitor
13	3.3V I/O	GPIO12	I/O	General purpose input/output 12
		ANA_IN12	AI	Analog input channel 12
		PWM_SOC	O	PWM_SOC output monitor, which is the logical OR of PWM_SOCA, PWM_SOCB, PWM_SOCC
14	3.3V I/O	GPIO13	I/O	General purpose input/output 13
		ANA_IN13	AI	Analog input channel 13
		CLKDET_DCLK	O	CLKDET detected clock output monitor
15	3.3V supply	AVDD	P	Analog supply Put 4.7uF and 0.1uF capacitor to AVSS
16	Ground	AVSS	G	Analog groud
17	3.3V I/O	GPIO14	I/O	General purpose input/output 14
		ANA_IN14	AI	Analog input channel 14
		COMP_MON0	O	Comparator output monitor0
18	3.3V I/O	GPIO15	I/O	General purpose input/output 15
		ANA_IN15	AI	Analog input channel 15

Pin	Type	Signal	Sub-type[1]	Description
19	3.3V I/O	GPIO16	I/O	General purpose input/output 16
		ANA_IN16	AI	Analog input channel 16
		UART2_TXD	O	UART2 transmitted data
		SPI0_MOSI	I/O	SPI0 data master output and slave input
		CAN0_TXD	O	CAN0 transmitted data
		ECAP0_APWM	O	ECAP0 APWM mode output
20	3.3V I/O	GPIO17	I/O	General purpose input/output 17
		ANA_IN17	AI	Analog input channel 17
		UART2_RXD	I	UART2 received data
		SPI0_MISO	I/O	SPI0 data master input and slave output
		CAN0_RXD	I	CAN0 received data
		ECAP1_APWM	O	ECAP1 APWM mode output
21	3.3V I/O	GPIO18	I/O	General purpose input/output 18
		ANA_IN18	AI	Analog input channel 18
		I2C0_SDA	I/O	I2C0 data input / output
		SPI0_SFRM	I/O	SPI0 frame signal input / output
		CAN1_TXD	O	CAN1 transmitted data
		ECAP2_APWM	O	ECAP2 APWM mode output
22	3.3V I/O	GPIO19	I/O	General purpose input/output 19
		ANA_IN19	AI	Analog input channel 19
		I2C0_SCL	I/O	I2C0 clock input / output
		SPI0_SCLK	I/O	SPI0 clock input / output
		CAN1_RXD	I	CAN1 received data
		ECAP3_APWM	O	ECAP3 APWM mode output
23	3.3V I/O	GPIO20	I/O	General purpose input/output 20
		ANA_IN20	AI	Analog input channel 20
		UART3_TXD	O	UART3 transmitted data
		SPI1_MOSI	I/O	SPI1 data master output and slave input
		EQEP0_A	I	EQEP0 quadrature signal A input
		ECAP4_APWM	O	ECAP4 APWM mode output
24	3.3V I/O	GPIO21	I/O	General purpose input/output 21
		ANA_IN21	AI	Analog input channel 21
		UART3_RXD	I	UART3 received data
		SPI1_MISO	I/O	SPI1 data master input and slave output
		EQEP0_B	I	EQEP0 quadrature signal B input
		ECAP5_APWM	O	ECAP5 APWM mode output
25	3.3V I/O	GPIO22	I/O	General purpose input/output 22
		ANA_IN22	AI	Analog input channel 22
		I2C1_SDA	I/O	I2C1 frame signal input / output
		SPI1_SFRM	I/O	SPI1 frame signal input / output
		EQEP0_Z	I	EQEP0 zero signal Z input
		ECAP6_APWM	O	ECAP6 APWM mode output
26	3.3V I/O	GPIO23	I/O	General purpose input/output 23
		ANA_IN23	AI	Analog input channel 23
		I2C1_SCL	I/O	I2C1 clock input / output
		SPI1_SCLK	I/O	SPI1 clock input / output

Pin	Type	Signal	Sub-type[1]	Description
		EQEP0_S	I	EQEP0 strobe signal S input
		ECAP7_APWM	O	ECAP7 APWM mode output
27	1.2V supply	VCAP12	P	1.2V supply **Put 2.2uF and 0.1uF capacitor to DVSS**
28	3.3V supply	DVDD	P	Digital supply **Put 4.7uF and 0.1uF capacitor to DVSS**
29	3.3V I/O	GPIO24	I/O	General purpose input/output 24
		XIN	AI	External crystal input
		I2C2_SDA	I/O	I2C2 data input / output
		COMP_MON2	O	Comparator output monitor2
		SYNC_MON0	O	Sync output monitor0
30	3.3V I/O	GPIO25	I/O	General purpose input/output 25
		XIO	AI/AO	External crystal input / output
		I2C2_SCL	I/O	I2C2 clock input / output
		SYNC_MON1	O	Sync output monitor1
31	3.3V I/O 5V tolerance	XRSTn	I	Reset pin, reset chip at low level. **Internal pull up to DVDD**
32	3.3V I/O 5V tolerance	GPIO36	I/O	General purpose input/output 36
		PWM0A	O	PWM0 output A
33	3.3V I/O 5V tolerance	GPIO37	I/O	General purpose input/output 37
		PWM0B	O	PWM0 output B
		PWM1A	O	PWM1 output A
34	3.3V I/O 5V tolerance	GPIO38	I/O	General purpose input/output 38
		PWM1A	O	PWM1 output A
		PWM2A	O	PWM2 output A
35	3.3V I/O 5V tolerance	GPIO39	I/O	General purpose input/output 39
		PWM1B	O	PWM1 output B
		PWM0B	O	PWM0 output B
36	3.3V I/O 5V tolerance	GPIO40	I/O	General purpose input/output 40
		PWM2A	O	PWM2 output A
		PWM1B	O	PWM1 output B
37	3.3V I/O 5V tolerance	GPIO41	I/O	General purpose input/output 41
		PWM2B	O	PWM2 output B
38	3.3V I/O 5V tolerance	GPIO46	I/O	General purpose input/output 46
		PWM3A	O	PWM3 output A
39	3.3V I/O 5V tolerance	GPIO47	I/O	General purpose input/output 47
		PWM3B	O	PWM3 output B
		PWM4A	O	PWM4 output A
40	3.3V I/O 5V tolerance	GPIO48	I/O	General purpose input/output 48
		PWM4A	O	PWM4 output A
		PWM5A	O	PWM5 output A
41	3.3V I/O 5V tolerance	GPIO49	I/O	General purpose input/output 49
		PWM4B	O	PWM4 output B
		PWM3B	O	PWM3 output B
42	3.3V I/O 5V tolerance	GPIO50	I/O	General purpose input/output 50
		PWM5A	O	PWM5 output A

Pin	Type	Signal	Sub-type[1]	Description
		PWM4B	O	PWM4 output B
43	3.3V I/O 5V tolerance	GPIO51	I/O	General purpose input/output 51
		PWM5B	O	PWM5 output B
44	3.3V I/O 5V tolerance	GPIO56	I/O	General purpose input/output 56
		PWM6A	O	PWM6 output A
		SPI2_MOSI	I/O	SPI2 data master output and slave input
		I2C0_SDA	I/O	I2C0 data input / output
		CAN0_TXD	O	CAN0 transmitted data
		EQEP1_A	I	EQEP1 quadrature signal A input
45	3.3V I/O 5V tolerance	GPIO57	I/O	General purpose input/output 57
		PWM6B	O	PWM6 output B
		PWM7A	O	PWM7 output A
		SPI2_MISO	I/O	SPI2 data master input and slave output
		I2C0_SCL	I/O	I2C0 clock input / output
		CAN0_RXD	I	CAN0 received data
		EQEP1_B	I	EQEP1 quadrature signal B input
46	3.3V I/O 5V tolerance	GPIO58	I/O	General purpose input/output 58
		PWM7A	O	PWM7 output A
		SPI2_SFRM	I/O	SPI2 frame signal input / output
		I2C1_SDA	I/O	I2C1 data input / output
		CAN1_TXD	O	CAN1 transmitted data
		EQEP1_Z	I	EQEP1 zero signal Z input
47	3.3V I/O 5V tolerance	GPIO59	I/O	General purpose input/output 59
		PWM7B	O	PWM7 output B
		PWM6B	O	PWM6 output B
		SPI2_SCLK	I/O	SPI2 clock input / output
		I2C1_SCL	I/O	I2C1 clock input / output
		CAN1_RXD	I	CAN1 received data
		EQEP1_S	I	EQEP1 strobe signal S input
48	3.3V I/O 5V tolerance	GPIO62	I/O	General purpose input/output 62
		UART0_TXD	O	UART0 transmitted data
		CAN0_TXD	O	CAN0 transmitted data
		SYNC_MON2	O	Sync output monitor2
		I2C0_SDA	I/O	I2C0 data input / output
49	3.3V I/O 5V tolerance	GPIO63	I/O	General purpose input/output 63
		UART0_RXD	I	UART0 received data
		CAN0_RXD	I	CAN0 received data
		SYNC_MON3	O	Sync output monitor3
		I2C0_SCL	I/O	I2C0 clock input / output
50	1.2V supply	VCAP12	P	1.2V supply **Put 0.1uF capacitor to DVSS**
51	3.3V supply	DVDD	P	Digital supply **Put 0.1uF bypass capacitor to DVSS**
52	3.3V I/O 5V tolerance	GPIO77	I/O	General purpose input/output 77
		UART1_RXD	I	UART1 received data
		CAN0_RXD	I	CAN0 received data

Pin	Type	Signal	Sub-type[1]	Description
		SYNC_MON5	O	Sync output monitor5
		CAN1_RXD	I	CAN1 received data
		I2C1_SCL	I/O	I2C1 clock input / output
53	3.3V I/O 5V tolerance	GPIO78	I/O	General purpose input/output 78
		UART1_TXD	O	UART1 transmitted data
		CAN0_TXD	O	CAN0 transmitted data
		COMP_MON4	O	Comparator output monitor4
		CAN1_TXD	O	CAN1 transmitted data
		I2C1_SDA	I/O	I2C1 data input / output
		EQEP0_A	I	EQEP0 quadrature signal A input
		Note: When TRSTn is high, the pin function is defined in Table 2-1.		
54	3.3V I/O 5V tolerance	GPIO79	I/O	General purpose input/output 79
		UART1_RXD	I	UART1 received data
		CAN0_RXD	I	CAN0 received data
		CAN1_RXD	I	CAN1 received data
		I2C1_SCL	I/O	I2C1 clock input / output
		EQEP0_B	I	EQEP0 quadrature signal B input
		Note: When TRSTn is high, the pin function is defined in Table 2-1.		
55	3.3V I/O 5V tolerance	GPIO80	I/O	General purpose input/output 80
		PWM_SOCA	O	PWM_SOCA output monitor
		PWM_SOCB	O	PWM_SOCB output monitor
		COMP_MON6	O	Comparator output monitor6
		SYNC_MON4	O	Sync output monitor4
		EQEP0_Z	I	EQEP0 zero signal Z input
		Note: When TRSTn is high, the pin function is defined in Table 2-1.		
56	3.3V I/O 5V tolerance	GPIO81	I/O	General purpose input/output 81
		PWM_SOCC	O	PWM_SOCC output monitor
		PWM_SOC	O	PWM_SOC output monitor, which is the logical OR of PWM_SOCA, PWM_SOCB, PWM_SOCC
		SYNC_MON5	O	Sync output monitor5
		EQEP0_S	I	EQEP0 strobe signal S input
		Note: When TRSTn is high, the pin function is defined in Table 2-1.		

[1] I = Digital input, O = Digital output, AI = Analog input, AO = Analog output, P = Power supply, G = Ground.

3.2 GPIO pin function and state after reset

Table 3-2: GPIO pin function and state after reset（SPC1185Z）

Pin Name	Default Function	Default State	Pin Name	Default function	Default state
–	–	–	GPIO1	ANA_IN1	Floating
GPIO2	ANA_IN2	Floating	GPIO3	ANA_IN3	Floating
GPIO4	ANA_IN4	Floating	GPIO5	ANA_IN5	Floating
GPIO6	ANA_IN6	Floating	GPIO7	ANA_IN7	Floating
GPIO8	ANA_IN8	Floating	GPIO9	ANA_IN9	Floating
GPIO10	ANA_IN10	Floating	GPIO11	ANA_IN11	Floating
GPIO12	ANA_IN12	Floating	GPIO13	ANA_IN13	Floating
GPIO14	ANA_IN14	Floating	GPIO15	ANA_IN15	Floating
GPIO16	ANA_IN16	Floating	GPIO17	ANA_IN17	Floating
GPIO18	ANA_IN18	Floating	GPIO19	ANA_IN19	Floating
GPIO20	ANA_IN20	Floating	GPIO21	ANA_IN21	Floating
GPIO22	ANA_IN22	Floating	GPIO23	ANA_IN23	Floating
GPIO24	GPIO24	Pull-up	GPIO25	GPIO25	Pull-up
GPIO36	GPIO36	Floating	GPIO37	GPIO37	Floating
GPIO38	GPIO38	Floating	GPIO39	GPIO39	Floating
GPIO40	GPIO40	Floating	GPIO41	GPIO41	Floating
GPIO46	GPIO46	Floating	GPIO47	GPIO47	Floating
GPIO48	GPIO48	Floating	GPIO49	GPIO49	Floating
GPIO50	GPIO50	Floating	GPIO51	GPIO51	Floating
GPIO56	GPIO56	Floating	GPIO57	GPIO57	Floating
GPIO58	GPIO58	Floating	GPIO59	GPIO59	Floating
GPIO62	GPIO62	Pull-up	GPIO63	GPIO63	Pull-up
–	–	–	GPIO77	GPIO77	Pull-up
GPIO78	GPIO78	Pull-up	GPIO79	GPIO79	Pull-up
GPIO80	GPIO80	Pull-up	GPIO81	GPIO81	Pull-up

3.3 ADC input channel selection

Table 3-3: ADC input channel selection

Option	ADC0		ADC1		ADC2	
	SHINSELP	SHINSELN	SHINSELP	SHINSELN	SHINSELP	SHINSELN
0	AVSS	AVSS	AVSS	AVSS	AVSS	AVSS
1	PGA0_OUTP	PGA0_OUTN	PGA1_OUTP	PGA1_OUTN	PGA2_OUTP	PGA2_OUTN
2	DAC0	DAC1	DAC2	DAC3	DAC4	DAC5
3	AVDD	VCAP12	ATEST	DACBUF0	TSENSOR_P	TSENSOR_N
4	–	ANA_IN1	ANA_IN2	ANA_IN3	ANA_IN4	ANA_IN5
5	ANA_IN6	ANA_IN7	ANA_IN8	ANA_IN9	ANA_IN10	ANA_IN11
6	ANA_IN12	ANA_IN13	ANA_IN14	ANA_IN15	ANA_IN16	ANA_IN17
7	ANA_IN18	ANA_IN19	ANA_IN20	ANA_IN21	ANA_IN22	ANA_IN23

3.4 PGA input channel selection

Table 3-4: PGA input channel selection

Option	PGA0		PGA1		PGA2	
	INSELP	INSELN	INSELP	INSELN	INSELP	INSELN
0	DAC5	DAC5	DAC5	DAC5	DAC5	DAC5
1	ANA_IN15	DAC0	ANA_IN18	DAC2	ANA_IN14	DAC4
2	ANA_IN4	ANA_IN10	ATEST	ANA_IN6	ANA_IN18	ANA_IN20
3	ANA_IN8	ANA_IN17	ANA_IN4	ANA_IN17	ANA_IN8	DACBUF1
4	–	ANA_IN1	ANA_IN2	ANA_IN3	ANA_IN4	ANA_IN5
5	ANA_IN6	ANA_IN7	ANA_IN8	ANA_IN9	ANA_IN10	ANA_IN11
6	ANA_IN12	ANA_IN13	ANA_IN14	ANA_IN15	ANA_IN16	ANA_IN17
7	ANA_IN18	ANA_IN19	ANA_IN20	ANA_IN21	ANA_IN22	ANA_IN23

3.5 Analog comparator input channel selection

Table 3-5: COMP0H/COMP0L input channel selection

INSEL	Input signal	REFSEL	PHCMPEN = 1	PHCMPEN = 0	
			COMP0H/L reference	COMP0H reference	COMP0L reference
0	PGA0_OUTN	0	PGA0_OUTP	DAC0	DAC1
1	ANA_IN4	1	ANA_IN7	DAC1	DAC0
2	ANA_IN5	2	ANA_IN8	DAC4	DAC5
3	ANA_IN6	3	ANA_IN9	DAC5	DAC4

Table 3-6: COMP1H/COMP1L input channel selection

INSEL	Input signal	REFSEL	PHCMPEN = 1	PHCMPEN = 0	
			COMP1H/L reference	COMP1H reference	COMP1L reference
0	PGA1_OUTN	0	PGA1_OUTP	DAC0	DAC1
1	ANA_IN10	1	ANA_IN13	DAC1	DAC0
2	ANA_IN11	2	ANA_IN14	DAC4	DAC5
3	ANA_IN12	3	ANA_IN15	DAC5	DAC4

Table 3-7: COMP2H/COMP2L input channel selection

INSEL	Input signal	REFSEL	PHCMPEN = 1	PHCMPEN = 0	
			COMP2H/L reference	COMP2H reference	COMP2L reference
0	PGA2_OUTN	0	PGA2_OUTP	DAC0	DAC1
1	ANA_IN16	1	ANA_IN19	DAC1	DAC0
2	ANA_IN17	2	ANA_IN20	DAC4	DAC5
3	ANA_IN18	3	ANA_IN21	DAC5	DAC4

Table 3-8: COMP3H/COMP3L input channel selection

INSEL	Input signal	REFSEL	PHCMPEN = 1	PHCMPEN = 0	
			COMP3H/L reference	COMP3H reference	COMP3L reference
0	PGA0_OUTP	0	PGA0_OUTN	DAC2	DAC3
1	ANA_IN6	1	ANA_IN5	DAC3	DAC2
2	ANA_IN8	2	ANA_IN7	DAC4	DAC5
3	ANA_IN10	3	ANA_IN9	DAC5	DAC4

Table 3-9: COMP4H/COMP4L input channel selection

INSEL	Input signal	REFSEL	PHCMPEN = 1	PHCMPEN = 0	
			COMP4H/L reference	COMP4H reference	COMP4L reference
0	PGA1_OUTP	0	PGA1_OUTN	DAC2	DAC3
1	ANA_IN12	1	ANA_IN11	DAC3	DAC2
2	ANA_IN14	2	ANA_IN13	DAC4	DAC5
3	ANA_IN16	3	ANA_IN15	DAC5	DAC4

Table 3-10: COMP5H/COMP5L input channel selection

INSEL	Input signal	REFSEL	PHCMPEN = 1	PHCMPEN = 0	
			COMP5H/L reference	COMP5H reference	COMP5L reference
0	PGA2_OUTP	0	PGA2_OUTN	DAC2	DAC3
1	ANA_IN18	1	ANA_IN17	DAC3	DAC2
2	ANA_IN20	2	ANA_IN19	DAC4	DAC5
3	ANA_IN22	3	ANA_IN21	DAC5	DAC4

Table 3-11: COMP6H/COMP6L input channel selection

INSEL	Input signal	REFSEL	PHCMPEN = 1	PHCMPEN = 0	
			COMP6H/L reference	COMP6H reference	COMP6L reference
0	ANA_IN2	0	ANA_IN3	DAC0	DAC1
1	ANA_IN8	1	ANA_IN9	DAC1	DAC0
2	ANA_IN10	2	ANA_IN11	DAC4	DAC5
3	ANA_IN12	3	ANA_IN13	DAC5	DAC4

Table 3-12: COMP7H/COMP7L input channel selection

INSEL	Input signal	REFSEL	PHCMPEN = 1	PHCMPEN = 0	
			COMP7H/L reference	COMP7H reference	COMP7L reference
0	–	0	ANA_IN1	DAC2	DAC3
1	ANA_IN21	1	ANA_IN19	DAC3	DAC2
2	ANA_IN20	2	ANA_IN18	DAC4	DAC5
3	ANA_IN22	3	ANA_IN23	DAC5	DAC4

3.6 Sync output monitor channel selection

Table 3-13: SYNC_MONx signal source

SYNCMONCTL.SRCx	SYNC_MONx	SYNCMONCTL.SRCx	SYNC_MONx
0	ECAP0_SYNCO [1]	8	EQEP0_SYNCO
1	ECAP1_SYNCO [1]	9	EQEP1_SYNCO
2	ECAP2_SYNCO [1]	10	TIMER0_SYNCO [1]
3	ECAP3_SYNCO [1]	11	TIMER1_SYNCO [1]
4	ECAP4_SYNCO [1]	12	TIMER2_SYNCO [1]
5	ECAP5_SYNCO [1]	13	TIMER3_SYNCO [1]
6	ECAP6_SYNCO [1]	14	TIMER4_SYNCO [1]
7	ECAP7_SYNCO [1]	15	PWM_SYNCO

[1] Pulse with is one functional clock cycle without extension, which is used only for function debug at low clock frequency.

3.7 Comparison output monitor channel selection

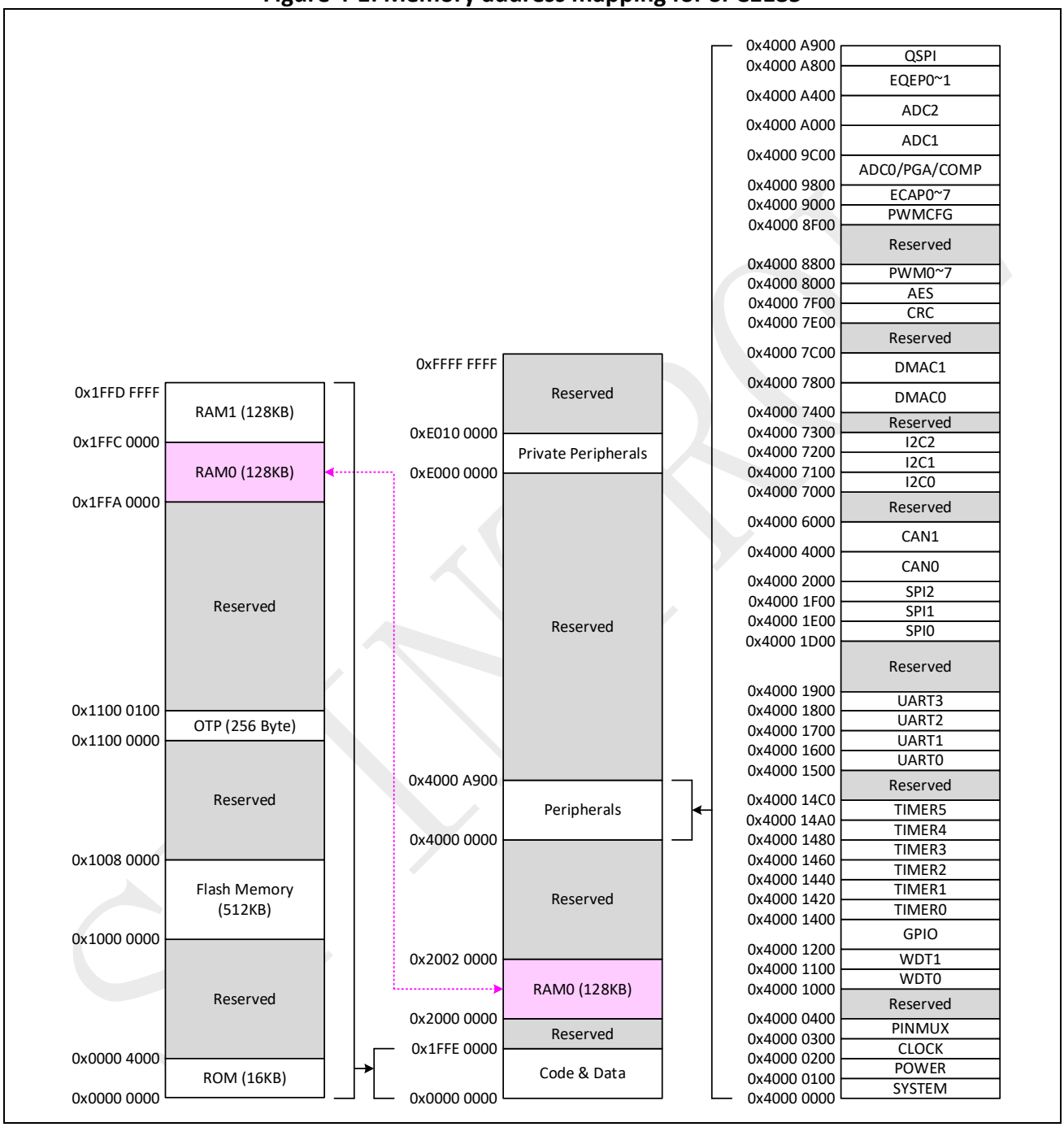
Table 3-14: COMP_MONx signal source (x = 0/2/4/6)

COMPMONCTL.SRCx	COMP_MONx	COMPMONCTL.SRCx	COMP_MONx
0	COMP0L	8	COMP4L
1	COMP0H	9	COMP4H
2	COMP1L	10	COMP5L
3	COMP1H	11	COMP5H
4	COMP2L	12	COMP6L
5	COMP2H	13	COMP6H
6	COMP3L	14	COMP7L
7	COMP3H	15	COMP7H

4 Memory address mapping

Memory address mapping for SPC1185 is shown in Figure 4-1.

Figure 4-1: Memory address mapping for SPC1185



5 Electrical characteristics

5.1 Absolute maximum ratings

Table 5-1: Absolute maximum ratings [1][2]

Symbol	Parameter	Min	Max	Unit
V_{DVDD}	Digital power supply, referred to V_{DVSS}	-0.3	4.6	V
V_{AVDD}	Analog power supply, referred to V_{AVSS}	-0.3	4.6	V
V_{IN}	Input voltage for 3.3V I/O (V_{DVDD}=3.3V)	-0.3	4.6	V
$V_{IN(5T)}$	Input voltage for 5V tolerant I/O (V_{DVDD}=3.3V)	-0.3	5.5	V
V_O	Output voltage	-0.3	4.6	V
I_{IC}	Input clamp current	-20	20	mA
I_{OC}	Output clamp current	-20	20	mA
T_J	Junction temperature [3]	-40	+125	°C
T_A	Ambient temperature [3]	-40	+105	°C
T_{stg}	Storage temperature [3]	-65	+150	°C

[1] Stress beyond the listed ratings may cause permanent damage to the device. These values are only the maximum ratings and do not imply that the device will function properly under these conditions.

[2] Unless otherwise specified, all voltages are referred to V_{DVSS}.

[3] Long-term storage at high temperatures or usage under maximum temperature conditions may reduce the lifetime of the device.

5.2 Recommended operating conditions

Table 5-2: Recommended operating conditions

Symbol	Parameter	Conditions	Min	Nom	Max	Unit
V_{DVDD}	Digital power supply	–	2.97	3.3	3.63	V
V_{DVSS}	Digital ground	–	–	0	–	V
V_{AVDD}	Analog power supply	–	2.97	3.3	3.63	V
V_{AVSS}	Analog ground	–	–	0	–	V
V_{IH}	High-level input voltage	V_{DVDD} = 3.3 V	2.0	–	V_{DVDD}+0.3	V
$V_{IH(5T)}$	High-level input voltage for 5V tolerant I/O	V_{DVDD} = 3.3 V	2.0	–	5	V
I_{OH}	High-level output source current when V_{OH}=$V_{OH(MIN)}$	STRENGTH=0 STRENGTH=1 STRENGTH=2 STRENGTH=3	–	–	5 10 15 20	mA
I_{OL}	Low-level output sink current when V_{OL}=$V_{OL(MAX)}$	STRENGTH=0 STRENGTH=1 STRENGTH=2 STRENGTH=3	–	–	5 10 15 20	mA
T_J	Junction temperature	–	-40	–	+125	°C
T_A	Ambient temperature	–	-40	–	+105	°C

5.3 I/O electrical characteristics

Table 5-3: I/O electrical characteristics

Symbol	Parameter	Conditions	Min	Nom	Max	Unit
V_{OH}	High-level output voltage	$I_{OH}=I_{OH(MAX)}$	V_{DVDD}-0.4	–	–	V
V_{OL}	Low-level output voltage	$I_{OL}=I_{OL(MAX)}$	–	0	0.4	V
V_{IH}	High-level input voltage	V_{DVDD}=3.3V	2.0	–	V_{DVDD}+0.3	V
$V_{IH(5T)}$	High-level input voltage for 5V tolerant I/O	V_{DVDD} = 3.3 V	2.0	–	5	V
V_{IL}	Low-level input voltage	V_{DVDD}=3.3V	V_{DVSS}-0.3	–	0.8	V
I_{OH}	High-level output source current when $V_{OH}=V_{OH(MIN)}$	STRENGTH=0 STRENGTH=1 STRENGTH=2 STRENGTH=3	–	–	5 10 15 20	mA
I_{OL}	Low-level output sink current when $V_{OL}=V_{OL(MAX)}$	STRENGTH=0 STRENGTH=1 STRENGTH=2 STRENGTH=3	–	–	5 10 15 20	mA
I_{IL}	Low-level input current (Disable pull-up/pull-down)	V_{DVDD}=3.3V V_{IN}=0V	–	–	10	uA
I_{IH}	High-level input current (Disable pull-up/pull-down)	V_{DVDD}=3.3V V_{IN}=3.3V	–	–	10	uA
R_{PU}	Input pull-up resistor	V_{IN}=0V	–	42	–	kΩ
R_{PD}	Input pull-down resistor	$V_{IN}=V_{DVDD}$	–	44	–	kΩ

5.4 Power consumption

Table 5-4: Power consumption (V_{DVDD}=3.3V) [1]

Mode	Junction temperature (T_J)					Unit
	T_J = -40 °C	T_J = 25 °C	T_J = 85 °C	T_J = 105 °C	T_J = 125 °C	
Active @ 240MHz (Run in Flash)	155	162	171	182	206	mA
Active @ 240MHz (Run in RAM)	177	181	191	205	225	mA
Active @ 32MHz (Run in Flash)	66	76	80	92	113	mA
Active @ 32MHz (Run in RAM)	67	73	77	90	108	mA
Stop	1.10	2.31	13.8	23.0	36.4	mA
Sleep	14.7	1.79	2.25	3.01	5.41	uA

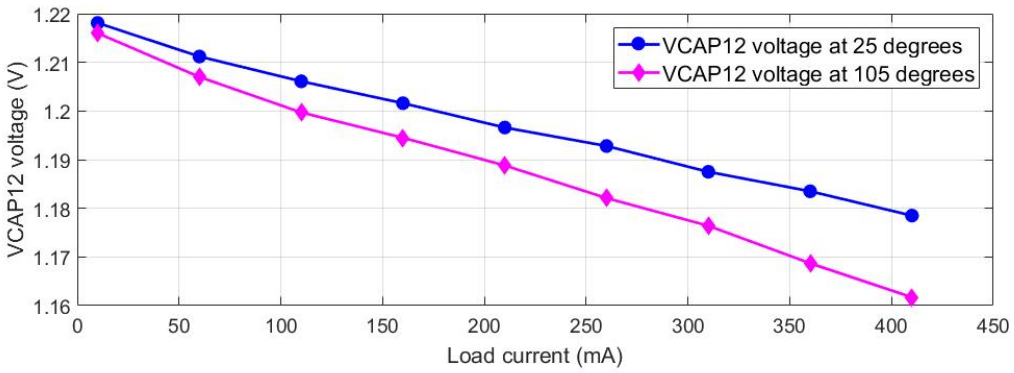
[1] Typical value of the maximum working condition.

5.5 Internal 1.2V LDO characteristics

Table 5-5: Internal 1.2V LDO characteristics

Symbol	Parameter	Conditions	Min	Typ	Max	Unit
V_{DVDD}	Supply voltage	–	2.97	3.3	3.63	V
V_{VCAP12}	Output voltage	Load current = 100mA	1.18	1.20	1.22	V
ΔVCAP12	Load regulation	V_{VCAP12}@50mA - V_{VCAP12}@200mA	–	–	30	mV

Figure 5-1: Internal 1.2V LDO load regulation



5.6 BOD characteristics

Table 5-6: BOD characteristics

Symbol	Parameter	Conditions	Min	Typ	Max	Unit
$V_{th1(VDD33OV)}$	3.3V supply over-voltage assert threshold	–	–	4.21	–	V
$V_{th0(VDD33OV)}$	3.3V supply over-voltage release threshold	–	–	4.05	–	V
$V_{th1(VDD33UV)}$	3.3V supply under-voltage assert threshold	–	–	2.56	–	V
$V_{th0(VDD33UV)}$	3.3V supply under-voltage release threshold	–	–	2.63	–	V
$V_{th1(VDD12OV)}$	1.2V supply over-voltage assert threshold	–	–	1.47	–	V
$V_{th0(VDD12OV)}$	1.2V supply over-voltage release threshold	–	–	1.45	–	V
$V_{th1(VDD12UV)}$	1.2V supply under-voltage assert threshold	–	–	0.94	–	V
$V_{th0(VDD12UV)}$	1.2V supply under-voltage release threshold	–	–	0.96	–	V

5.7 RCO characteristics

Table 5-7: RCO characteristics

Symbol	Parameter	Conditions	Min	Typ	Max	Unit
f_{RCO}	RCO frequency	T_J = 25°C	–	32	–	MHz
E_{RCO} [1]	RCO frequency error	T_J = -40°C ~ 125°C	-1	–	1	%
t_{settle} [1]	RCO clock settling time	Settle to E_{RCO} < 1%	–	4.3	–	us

[1] Design guarantee without manufacture test

5.8 PLL characteristics

Table 5-8: PLL characteristics

Symbol	Parameter	Conditions	Min	Typ	Max	Unit
f_{VCO}	VCO frequency	–	400	–	600	MHz
f_{PFD}	PFD input frequency	–	4	–	8	MHz
t_{settle}	Settling time	Frequency error < 0.1%	–	–	15	us

5.9 XO characteristics

Table 5-9: XO characteristics

Symbol	Parameter	Conditions	Min	Typ	Max	Unit
f_{XO}	External crystal frequency	–	4	–	32	MHz

5.10 14-bit ADC characteristics

Table 5-10: ADC characteristics

Symbol	Parameter	Conditions	Min	Typ	Max	Unit
N_R	Resolution	Monotonic w/o missing code	–	14	–	bit
t_{sample}	Sampling time	–	–	140	–	ns
$t_{convert}$	Conversion time	–	140	–	–	ns
V_{in}	Input voltage range	–	0	–	V_{AVDD}	V
V_{ref}	Reference voltage	–	1.194	1.2	1.206	V
I_{on}	Operation current	V_{AVDD}= 3.3 V	–	12	16.5	mA
INL	Integral non-linearity	–	-3.0	–	3.0	LSB
DNL	Differential non-linearity	–	-1.0	–	1.0	LSB
E_{offset}	Offset error [1]	After calibration	-8	±2	8	LSB
E_{gain}	Gain error [1]	After calibration	-60	±4	60	LSB
T_{coef}	Temperature coefficient based on internal reference	–	–	40	–	ppm/°C
t_{settle} [2]	Power up settling time	–	–	–	100	us
$ENOB_{DC}$	Effective number of bits (DC input)	–	–	12.2	–	bit
SNR	Signal-to-noise ratio	f_{in} = 100kHz V_{in} = 0.94FS N = 8192	–	74	–	dBFS
THD	Total harmonic distortion		–	-87	–	dBFS
ENOB	Effective number of bits		–	12.0	–	bit
SFDR	Spurious free dynamic range		–	83	–	dBFS
T_{slope}	Temperature variance corresponding to 1LSB of ADC code	–	–	1.732	–	°C/LSB
T_{offset}	ADC code for temperature sensor @ 25°C	–	–	176.858	–	LSB

[1] Offset and gain error can be automatically corrected by hardware.
[2] Design guarantee without manufacture test

5.11 PGA characteristics

Table 5-11: PGA characteristics

Symbol	Parameter	Conditions	Min	Typ	Max	Unit
V_{in}	Input voltage range	–	0	–	V_{AVDD}	V
V_{out}	Output voltage range	–	0.3	–	V_{AVDD}-0.3	V
R_{in}	Input impedance	–	–	10	–	MΩ
G	Gain	MODE = 3 (Differential sensor) MODE = 5, 6, 7 (Single-ended)	1, 2, 4, 8, 12, 16, 24, 32			–
		MODE = 1, 2(Differential motor)	2, 4, 8, 16, 24, 32, 48, 64			–
E_{gain}	Gain error	Differential gain = 2	-0.5	–	0.5	%
		Differential gain = 64	-3	–	3	%
V_{offset}	Offset	Differential gain = 64	-5	–	5	mV
T_{coef}	Offset drift over temperature	–	–	5	–	uV/°C
SR	Slew rate	Single-ended and loaded by ADC sampling capacitor	–	20	–	V/us
		Differential-ended and loaded by ADC sampling cap	–	40	–	V/us
GBW	Gain-bandwidth product	Single-ended gain = 1	–	40	–	MHz
		Single-ended gain = 8	–	6.8	–	MHz
		Single-ended gain = 32	–	1.7	–	MHz
		Differential gain = 2	–	20	–	MHz
		Differential gain = 16	–	3.4	–	MHz
		Differential gain = 64	–	0.8	–	MHz
t_{settle}	Settling time [1]	Differential gain = 2	–	170	220	ns
		Differential gain = 16	–	400	600	ns
		Differential gain = 64	–	1600	2200	ns
SNR	Signal-to-noise ratio	Differential gain = 4 f_{in} = 10kHz, V_{in} = 0.94FS, N = 8192	–	71.0	–	dBFS
THD	Total harmonic distortion		–	-80.0	–	dBFS
ENOB	Effective number of bits		–	11.5	–	bit
SFDR	Spurious free dynamic range		–	81.5	–	dBFS
SNR	Signal-to-noise ratio	Differential gain = 64 f_{in} = 10kHz V_{in} = 0.94FS N = 8192	–	58.0	–	dBFS
THD	Total harmonic distortion		–	-80.0	–	dBFS
ENOB	Effective number of bits		–	9.4	–	bit
SFDR	Spurious free dynamic range		–	63.0	–	dBFS
I_{on}	Operation current	Single PGA	–	4.16	5.20	mA

[1] The settling time is defined as the time required for the differential output to be settled to 98% from -2.7V to 2.7V (V_{AVDD}=3.3V) upon a step input. It is guaranteed by design without manufacture measurement.

5.12 Analog comparator characteristics

Table 5-12: Analog comparator characteristics

Symbol	Parameter	Condition	Min	Typ	Max	Unit
V_{in}	Input voltage range	–	0	–	V_{AVDD}	V
V_{offset}	Offset (Hysteresis option = 0)	V_{AVDD} = 3.3V，T_J = 25°C 1.65V common-mode input	-10	–	10	mV
V_{hyst}	Hysteresis option = 0		–	0	–	mV
	Hysteresis option = 1		–	13	–	mV
	Hysteresis option = 2		–	26	–	mV
	Hysteresis option = 3		–	42	–	mV
t_d	Latency from the comparator response to PWM shutdown. (Hysteresis option = 0)		–	–	50	ns

5.13 DAC characteristics

Table 5-13: 10-bit DAC characteristics

Symbol	Parameter	Condition	Min	Typ	Max	Unit
N	Resolution	Monotonic	–	10	–	bit
V_{FS}	Full scale	–	0	–	V_{AVDD}	V
DNL	Differential non-linearity	–	-0.5	–	0.5	LSB
INL	Integral non-linearity	–	-1	–	1	LSB
E_{offset}	Offset error	–	-10	–	10	mV
t_{settle}	Settling time	Error < 1/2 LSB	–	–	1	us

Table 5-14: 12-bit DAC characteristics

Symbol	Parameter	Condition	Min	Typ	Max	Unit
N	Resolution	Monotonic	–	12	–	bit
V_{FS}	Full scale	–	0	–	V_{AVDD}	V
DNL	Differential non-linearity	–	-0.5	–	0.5	LSB
INL	Integral non-linearity	–	-2	–	2	LSB
E_{offset}	Offset error	–	-5	–	5	mV
t_{settle}	Settling time	Error < 1/2 LSB	–	–	1	us

[1] The DAC is used to generate a static voltage as a threshold for the comparator and does not guarantee the performance of the waveform produced by dynamically changing the code value.

5.14 DAC buffer characteristics

Table 5-15: DAC buffer characteristics

Symbol	Parameter	Condition	Min	Typ	Max	Unit
V_{out}	Output voltage	–	0.3	–	V_{AVDD}-0.4	V
t_{settle}	Settling time	Error < 1/2 LSB	–	–	1	us
E_{offset}	Offset error	–	-5	–	5	mV
C_L	Capacitive load	–	–	–	50	pF
R_L	Resistive load	–	5	–	–	KΩ

5.15 SPI timing characteristics

Figure 5-2: SPI master timing diagram

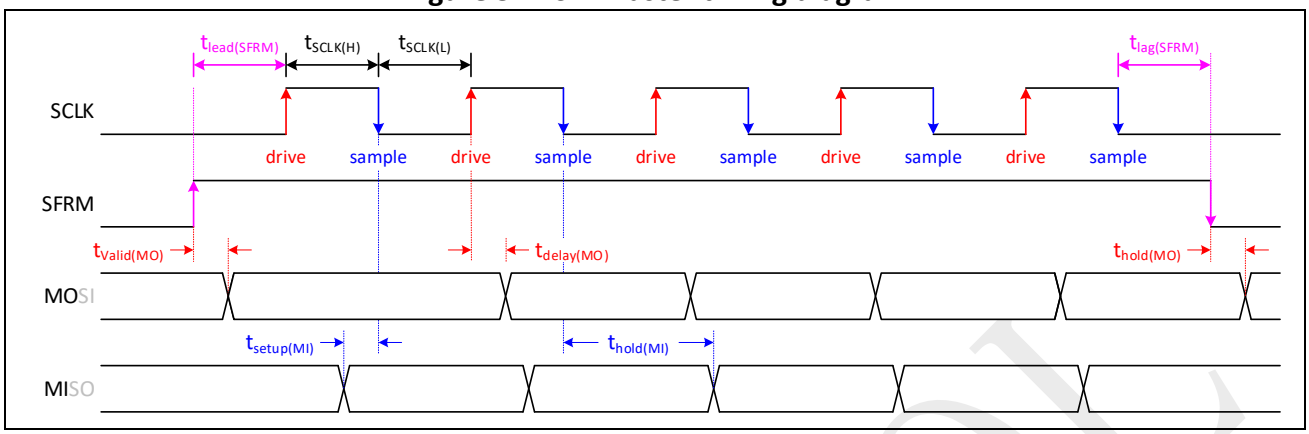


Table 5-16: SPI master timing characteristics (V_{DVDD}=3.3V)[1]

Symbol	Parameter	Condition	Min	Typ	Max	Unit
f_{SCLK}	SCLK clock frequency	15pF Pin capacitance	–	–	30	MHz
$t_{SCLK(H)}$	SCLK high-level time		16.6	–	–	ns
$t_{SCLK(L)}$	SCLK low-level time		16.6	–	–	ns
$t_{lead(SFRM)}$	Leading time of active SFRM edge before the first SCLK edge		t_{SCLK}/2-15	–	t_{SCLK}/2-1	ns
$t_{lag(SFRM)}$	Lagging time of inactive SFRM edge after the last SCLK edge		t_{SCLK}/2-0.5	–	t_{SCLK}/2+8	ns
$t_{valid(MO)}$	Latency from active SFRM edge to MOSI transition		-5	–	3	ns
$t_{hold(MO)}$	Latency from inactive SFRM edge to MOSI transition		-5	–	3	ns
$t_{delay(MO)}$	Latency from SCLK driving edge to MOSI transition		0.8	–	3	ns
$t_{setup(MI)}$	Setup time of MISO before SCLK sampling edge		8	–	–	ns
$t_{hold(MI)}$	Hold time of MISO after SCLK sampling edge		-2	–	–	ns

[1] Guaranteed by design.

Figure 5-3: SPI slave timing diagram

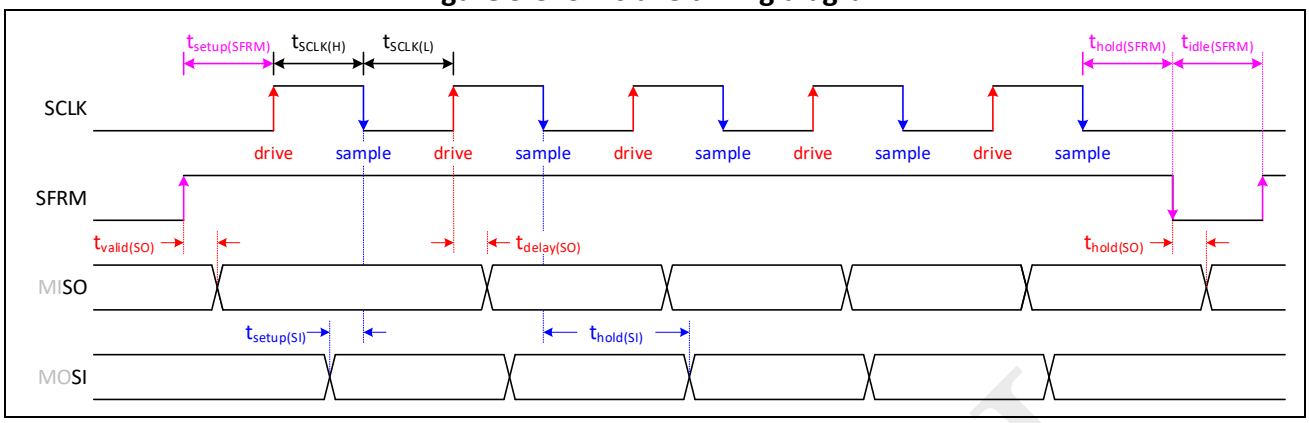


Table 5-17: SPI slave timing characteristics (V_{DVDD}=3.3V)[1]

Symbol	Parameter	Condition	Min	Typ	Max	Unit
f_{SCLK}	SCLK clock frequency	15pF Pin capacitance	–	–	30	MHz
$t_{SCLK(H)}$	SCLK high-level time		16.6	–	–	ns
$t_{SCLK(L)}$	SCLK low-level time		16.6	–	–	ns
$t_{idle(SFRM)}$	Inter-frame idle time when SFRM is at inactive level		4×t_{CLK_CPU}	–	–	ns
$t_{setup(SFRM)}$	Setup time of active SFRM before the first SCLK edge		10	–	–	ns
$t_{hold(SFRM)}$	Hold time of active SFRM after the last SCLK edge		10	–	–	ns
t_{valid}(SO)	Latency from SFRM active edge to MISO transition		4	–	10	ns
t_{hold}(SO)	Latency from SFRM inactive edge to MISO transition		4	–	10	ns
t_{delay}(SO)	Latency from SCLK driving edge to MISO transition		4	–	11	ns
t_{setup}(SI)	Setup time of MOSI before SCLK sampling edge		1	–	–	ns
t_{hold}(SI)	Hold time of MOSI after SCLK sampling edge		2	–	–	ns

[1] Guaranteed by design.

5.16 Electrical sensitivity characteristics

Table 5-18: ESD absolute maximum ratings

Symbol	Parameter	Condition		Max	Unit
$V_{ESD(HBM)}$	Electrostatic discharge voltage (Human body model)	Ambient temperature T_A = 25°C		4000	V
$V_{ESD(CDM)}$	Electrostatic discharge voltage (Charge device model)	Ambient temperature T_A = 25°C	–	500	V
			Corner Pin	750	V

Table 5-19: Electrical sensitivity

Symbol	Parameter	Condition	Max	Unit
LU	Static latch-up	Ambient temperature T_A = 105°C V_{DVDD} = V_{AVDD} = 3.63V	200	mA

5.17 Moisture sensitivity characteristics

Table 5-20: Moisture sensitivity characteristics

Symbol	Parameter	Condition	Max	Unit
MSL	Moisture sensitivity level	–	Level-3	–

5.18 Thermal resistance characteristics

Table 5-21: Thermal resistance characteristics (QFN56, 6mm x 6mm)

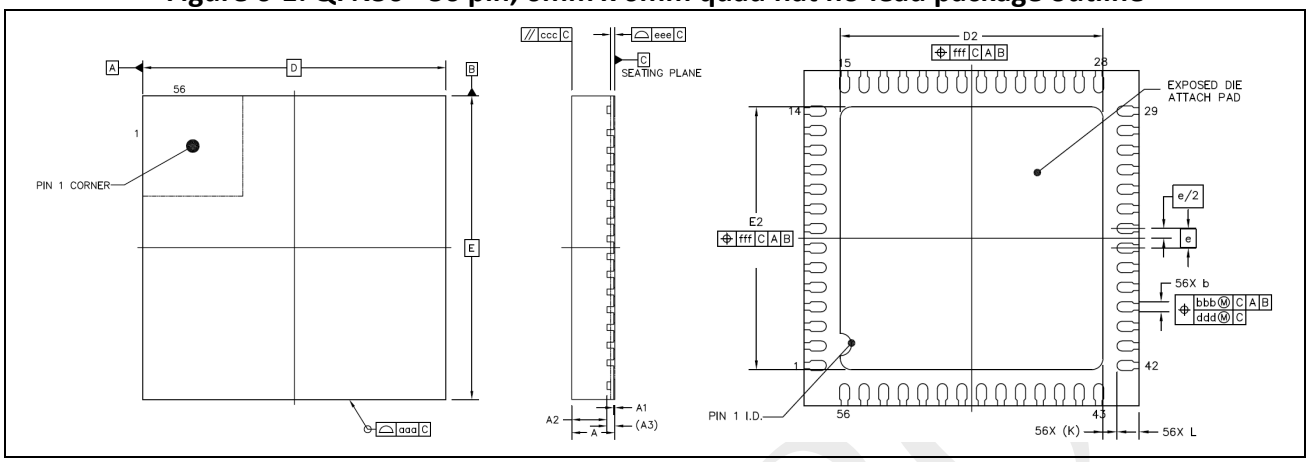
Symbol	Parameter	Condition	Typ	Unit
θ_{JC}	Junction-to-case thermal resistance	–	10.22	°C/W
θ_{JA}	Junction-to-ambient thermal resistance	Single-layer PCB. Copper content is 20%	57.25	°C/W
		4-layer PCB. Copper content from top to bottom is 20%, 100%, 100%, 5%	33.83	°C/W

[1] Dimension of PCB under test is 76.2mm x 114.3mm x 1.6mm.

6 Package information

6.1 QFN56（6mm x 6mm）

Figure 6-1: QFN56 - 56 pin, 6mm x 6mm quad flat no-lead package outline

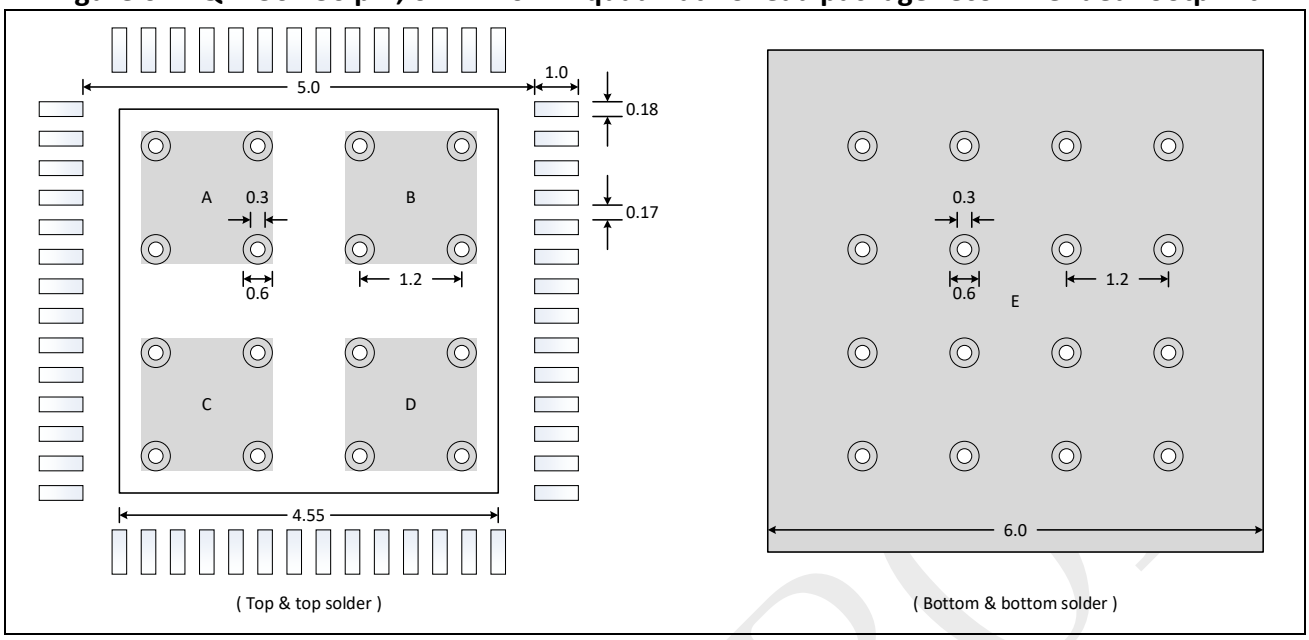


[1] Drawing is not to scale.

Table 6-1: QFN56 - 56 pin, 6mm x 6mm quad flat no-lead package mechanical data

Symbol	Dimension (mm)		
	Min	Typ	Max
A	0.80	0.85	0.90
A1	0	0.02	0.05
A2	–	0.7	–
A3		0.152 REF	
b	0.13	0.18	0.23
D		6 BSC	
E		6 BSC	
e		0.35 BSC	
D2	4.6	4.7	4.8
E2	4.6	4.7	4.8
L	0.3	0.4	0.5
K		0.25 REF	
aaa		0.1	
ccc		0.1	
eee		0.08	
bbb		0.07	
ddd		0.05	
fff		0.1	

Figure 6-2: QFN56 - 56 pin, 6mm x 6mm quad flat no-lead package recommended footprint



[1] Unit: mm

[2] Region A, B, C and D should be covered by solder paste, while region E has no special request.

7 Ordering information

Table 7-1: Ordering information

Ordering Number	Flash	SRAM	Max CPU Frequency	Package (mm)	Temperature range	SPQ[1]	Packing
SPC1185ZAPI56	512 KB	256 KB	240 MHz	QFN56 (6 x 6)	Industrial -40 °C~+125°C	4900	Tray

[1] SPQ = Standard Pack Quantity

7.1 Rule of ordering number

Figure 7-1: Rule of ordering number